This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A mixer circuit, comprising at least a differential pair transistors for inputting a first frequency signal or a second frequency signal and generating a third frequency signal by multiplying the first frequency signal and the second frequency signal, wherein each transistor of the differential pair transistors is a MIS transistor comprising:

a semiconductor substrate for comprising a first crystal plane as a principal plane;

a semiconductor structure, formed as a part of the semiconductor substrate, for comprising a pair of sidewall planes defined by the second crystal plane different from the first crystal plane and a top plane defined by the third crystal plane different from the second crystal plane;

a gate insulator of uniform thickness for covering the principal plane, the sidewall planes and the top plane;

a gate electrode for continuously covering the principal plane, the sidewall planes and the top plane on top of the gate insulator; and

a single conductivity type diffusion region formed in one side and the other side of the gate electrode in the semiconductor substrate and the semiconductor structure and continuously extending along the principal plane, the sidewall planes and the top plane.

2. (original) A mixer circuit, comprising at least a differential pair transistors for inputting a first frequency signal or a second frequency signal and generating a third frequency signal by multiplying the first frequency signal and the second frequency signal, wherein each transistor of the differential pair transistors is a MIS transistor comprising:

a semiconductor substrate comprising a projecting part, of which the surfaces are at least two different crystal planes on a principal plane;

a gate insulator for covering at least a part of each of said at least two different crystal planes constituting the surface of the projecting part;

a gate electrode comprised by the gate insulator so as to be electrically insulated from the semiconductor substrate, and comprised on each of said at least two different crystal planes constituting the surface of the projecting part; and

a single conductivity type diffusion region formed in the projecting part facing each of said at least two different crystal planes constituting the surface of the projecting part and individually formed in both side of the gate electrode.

3. (original) A mixer circuit, comprising at least a differential pair transistors for inputting a first frequency signal or a second frequency signal and generating a third frequency signal by multiplying the first frequency signal and the second frequency signal, wherein each transistor of the differential pair transistors is a three-dimensional MIS transistor, comprising:

a semiconductor substrate comprising at least two crystal planes;

a gate insulator formed on at least two of the crystal planes of the semiconductor substrate; and

a gate electrode formed on the semiconductor substrate sandwiching the gate insulator,

in which when voltage is applied to the gate electrode, a channel width of a channel formed in the semiconductor substrate along with the gate insulator is represented by summation of each channel width of the channels individually formed on said at least two crystal planes.

4. (currently amended) The mixer circuit according to ~~any of~~ claim 1 ~~to claim 3~~, wherein the MIS transistor is characterized in:

that the semiconductor substrate is a silicon substrate; and

that a gate insulator on a surface of the silicon substrate, is formed by removing hydrogen in such a way that the surface of the silicon substrate is exposed to plasma of a prescribed inert gas, and the hydrogen content at the interface of the silicon substrate and the gate insulator is $10^{11}/cm^2$ or less in units of surface density.

5. (currently amended) The mixer circuit according to claim ~~4~~ 2, wherein ~~said at least two crystal planes are any two different crystal planes from a (100) plane, a (110) plane and a (111) plane.~~ the MIS transistor is characterized in:

that the semiconductor substrate is a silicon substrate; and

that a gate insulator on a surface of the silicon substrate, is formed by removing hydrogen in such a way that the surface of the silicon substrate is exposed to plasma of a prescribed inert gas, and the hydrogen content at the interface of the silicon substrate and the gate insulator is $10^{11}/cm^2$ or less in units of surface density.

6. (currently amended) The mixer circuit according to claim ~~1~~ 3, wherein ~~the mixer circuit is a Gilbert cell type circuit.~~ the MIS transistor is characterized in:

that the semiconductor substrate is a silicon substrate; and

that a gate insulator on a surface of the silicon substrate, is formed by removing hydrogen in such a way that the surface of the silicon substrate is exposed to plasma of a prescribed inert gas, and the hydrogen content at the interface of the silicon substrate and the gate insulator is $10^{11}/cm^2$ or less in units of surface density.

7. (currently amended) The mixer circuit according to either claim ~~1 or claim 3~~ 4, wherein ~~the circuit configuration of the mixer circuit is using the MIS transistors symmetrically.~~ said at least two crystal planes are any two different crystal planes from a (100) plane, a (110) plane and a (111) plane.

8. (currently amended) The mixer circuit according to ~~either~~ claim 1 ~~or claim 3, used as a receiver for the first frequency signal, which is a high-frequency signal, the second frequency signal, which is a local signal, and the third frequency signal, which is a low-frequency signal.~~ wherein the mixer circuit is a Gilbert cell type circuit.

9. (currently amended) The mixer circuit according to claim ~~8~~ 1, wherein ~~the low-frequency signal is used in a direct conversion receiving system where the signal is a base band signal.~~ the circuit configuration of the mixer circuit is using the MIS transistors symmetrically.

10. (currently amended) A mixer circuit according to claim 3, ~~comprising a CMOS transistor configured in an n-channel MOS transistor and a p-channel MOS transistor,~~ wherein the circuit configuration of ~~at least one of the n-channel MOS transistor or the p-channel MOS transistor comprises the MIS transistor of~~ the mixer circuit is using the MIS transistors symmetrically ~~according to claim 1 or claim 3~~.

11. (currently amended) The mixer circuit according to claim ~~10~~ 1, ~~wherein element areas and current driving capacities of the p-channel MOS transistor and the n-channel MOS transistor closely agree with each other~~ used as a receiver for the first frequency signal,

which is a high-frequency signal, the second frequency signal, which is a local signal, and the third frequency signal, which is a low-frequency signal.

12. (new) The mixer circuit according to claim 3, used as a receiver for the first frequency signal, which is a high-frequency signal, the second frequency signal, which is a local signal, and the third frequency signal, which is a low-frequency signal.

13. (new) The mixer circuit according to claim 11, wherein the low-frequency signal is used in a direct conversion receiving system where the signal is a base band signal.

14. (new) A mixer circuit, comprising a CMOS transistor configured in an n-channel MOS transistor and a p-channel MOS transistor, wherein at least one of the n-channel MOS transistor or the p-channel MOS transistor comprises the MIS transistor of the mixer circuit according to claim 1.

15. (new) A mixer circuit, comprising a CMOS transistor configured in an n-channel MOS transistor and a p-channel MOS transistor, wherein at least one of the n-channel MOS transistor or the p-channel MOS transistor comprises the MIS transistor of the mixer circuit according to claim 3.

16. (new) The mixer circuit according to claim 14, wherein element areas and current driving capacities of the p-channel MOS transistor and the n-channel MOS transistor closely agree with each other.